MQ342-01

EPSON

Application Manual

Real Time Clock Module

RTC-4553AC

SEIKO EPSON CORPORATION

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Real-Time Clock Module

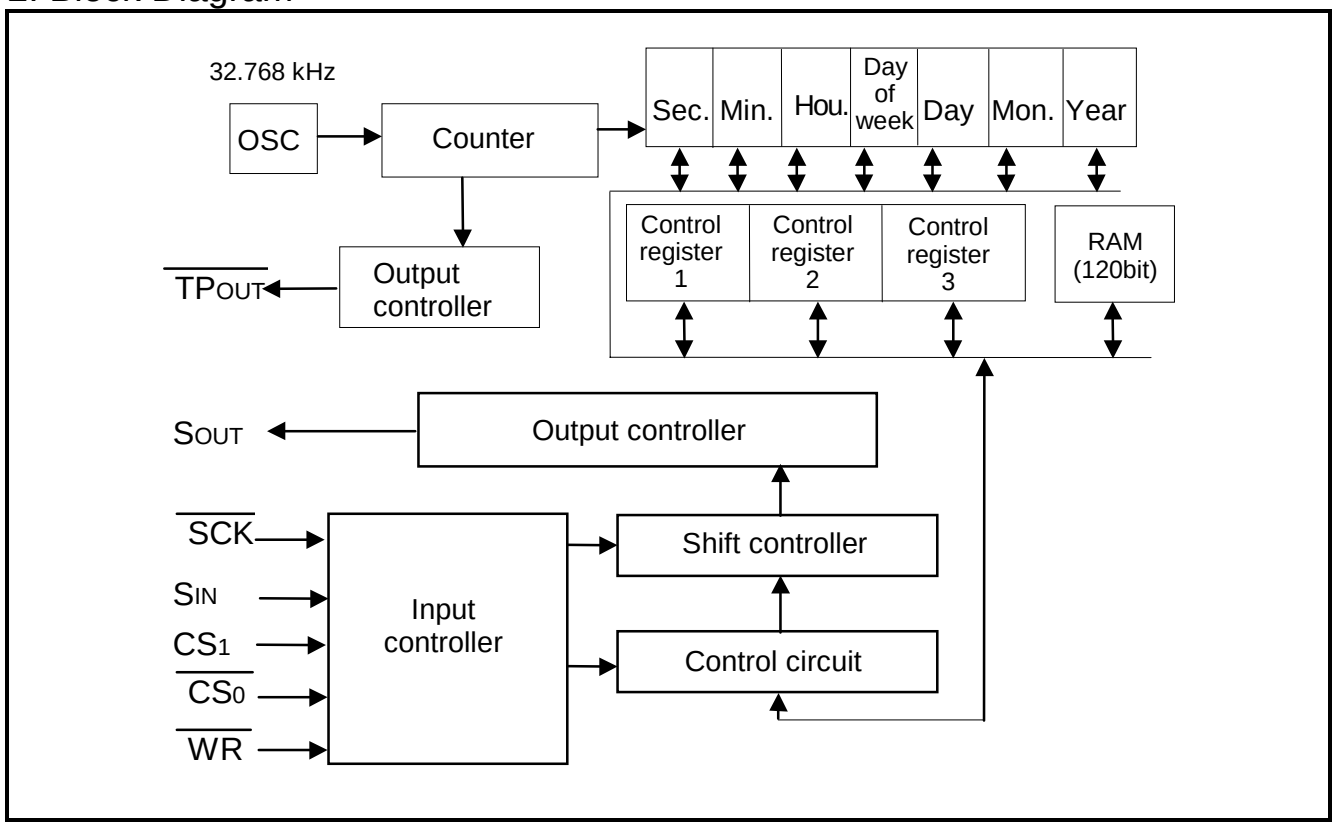
RTC – 4553AC

- Designed for E-mater
- Built-in 32.768 kHz quartz crystal allows adjustment- free operation and assures high accuracy
- Integrated clock (hours, minutes, seconds) and calendar (year, month, day, day of the week) counter
- Automatic leap year compensation until 2099
- Selectable 24-hour/12-hour display mode (with AM/PM indication)
- Clock data modification using increment method
- Clock data serial output in BCD format
- Software controlled 30 second adjustment
- Selectable 1/10 Hz or 1024 Hz timing pulse output
- Built-in SRAM (30 × 4 bit)
- Constant voltage drive realizes low power consumption (1 μA Typ.) and minimizes voltage-induced frequency fluctuations
- Supports low-voltage operation (3 V)

1. Overview

The RTC-4553 is a very compact real-time clock module with permanent calendar and serial data input/output. The module is designed for E-mater; time accuracy is within $\pm 5 \times 10^{-6}$ (±0.432 sec./day).
It incorporates a heat-resistant 32.768 kHz quartz oscillator. The space saving package allows high-density mounting and facilitates automated production.
Besides the clock and calendar functions (comprising all items from years to seconds), the RTC-4553 incorporates also a 30 × 4 bit SRAM and offers other useful features.
The use of a CMOS IC makes possible low-voltage, low-power operation, to ensure proper timekeeping also when powered from a backup battery.

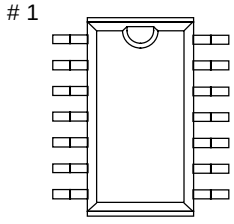
2. Block Diagram



3. Terminal description

3.1. Terminal connections

RTC - 4553



SOP - 14 pin

3.2. Terminal functions

Signal designation	Pin No.	Input / Output	Function
GND	1	—	Power supply negative pin. Connect to ground.
$\overline{WR}$ (WRITE enable)	2	I	Address and data are written at $\overline{WR}$ = "L". Counter data (second digit to year digit) are written using the incrementing method. Data at the specified address are read at $\overline{WR}$ = "H". While the address is being set at SIN, the data at SOUT are for the previously specified address.
SIN (Serial input)	3	I	Serial address and data I/O pin. Serves for address and control register writing for the various counters, and for RAM address and data writing.
$\overline{SCK}$ (Serial clock)	4	I	Serial I/O sync signal input pin. Input a sync signal to this pin to allow address and data read/write synchronized to this signal. One cycle comprises 8 clocks (4 address clocks + 4 data clocks)
L1–L3 L4 , L5	5–7 9, 10	—	Test pins reserved for use by Epson. Be sure to leave these pins unconnected.
VDD	8	—	Power supply pin. Connect to a power source. For normal operation and bus access, supply 5 V ±10% or 3 V ±10%. For backup battery operation, provide a voltage of 2 V or higher. See Note 1.
$\overline{CS0}$ (Chip select 0)	11	I	This pin serves to select the RTC. While $\overline{CS0}$ is "L", the microprocessor can perform register access. While $\overline{CS0}$ is "H", SOUT is in the high-impedance state.
$\overline{CS1}$ (Chip select 1)	12	I	Connect this pin to the power down detection circuit. If no power down detection circuit is used, fix the pin at "H" (VDD). When CS1 is "L", SOUT and $\overline{TPOUT}$ are in the high-impedance state, regardless of $\overline{CS0}$.
$\overline{SOUT}$ (Serial output)	13	O	Serial address and data output pin. Serves for address and control register readout of the various counters, and for RAM address and data readout.
$\overline{TPOUT}$ (Timing pulse output)	14	O	Output pin for 1024 Hz or 1/10 Hz timing pulse, based on internal reference clock. For clock accuracy checking, use 1/10 Hz. For 1024 Hz, the duty cycle changes once every 10 seconds.

Note1 At initial power-on or voltage restoration from an intermediate potential outside of the range where operation is assured (0.3 V to 1.9 V), the power-on reset circuit may not operate normally, leading to possible malfunction. (See section " 8.3.9. Power-On Reset ".)

Note2 Be sure to connect a bypass capacitor of 0.1 µF or more directly between VDD and GND.

4. Absolute maximum ratings

GND=0 V

Item	Symbol	Condition (pin)	Min.	Max.	Unit
Power supply voltage	V_{DD}	V_{DD}–GND	–0.3	+6.0	V
Input voltage	V_{IN}	SIN, $\overline{SCK}$, $\overline{WR}$, $\overline{CS0}$, CS1	–0.3	V_{DD}+0.3	
Output voltage	V_{OUT}	SOUT, $\overline{TP_{OUT}}$	–0.3	V_{DD}+0.3	
Storage temperature	T_{STG}	Stored bare product after unpacking	–55	+125	°C
Soldering conditions	T_{SOL}	—	Twice at under +260 °C within 10 seconds, or under +230 °C within 3 minutes		

5. Recommended operating conditions

GND=0 V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	V_{DD}–GND	2.7	5.0	5.5	V
Operation temperature	T_{OPR}	No condensation	–30	—	+70	°C

6. Frequency characteristics

GND=0 V

Item	Symbol	Condition		Rating	Unit
Frequency precision	$\Delta f / fo$	Ta = +25 °C V_{DD} = 5.0 V	AC	± 5	$\times 10^{-6}$
				± 0.432	sec. / day
Frequency/temperature characteristics	t_{OP}	Ta = –10 °C to +70 °C, V_{DD} = 5 V (Referenced at +25 °C)		+10 –120	$\times 10^{-6}$
Frequency/voltage characteristics	f / V	Ta = Fixed, V_{DD} = 2 V to 5.5 V (Referenced at 5 V)		± 5	$\times 10^{-6}$
Aging	fa	Ta = +25 °C, V_{DD} = 5 V, First year		± 5	$\times 10^{-6}$ / year

Note

(1) Frequency tolerance rating applies to V_{DD} = 5.0 V.
(At V_{DD} = 3 V, voltage characteristics must be taken into consideration.)

(2) Frequency tolerance rating applies at the time of shipment.

(3) Design the peripheral circuitry so that power start-up time (t_R) is 1.0 µs/V ≤ t_R ≤ 1.6 ms/V.

7. Electrical characteristics

7.1. DC, AC Characteristics

7.1.1. V_{DD} = 5 V

(1) DC Characteristics (GND=0 V , Ta = –30 °C ~ +70 °C)

Item	Symbol	Condition	V_{DD} = 5 V ± 10 %			Unit
			Min.	Typ.	Max.	
Data retention voltage	V_{DH}	—	2.0	—	5.5	V
Current consumption	$I_{DD}1$ (normal operation)	$\overline{SCK}$ = 500 kHz $\overline{CS0}$ = L, CS1 = H	—	—	100	µA
	$I_{DD}2$ (backup operation)	$\overline{SCK}$ = 0 Hz $\overline{CS0}$ = H, CS1 = L	—	1.0	3.0	
Output voltage	V_{OH}	I_{OH} = –400 µA	V_{DD} – 0.4	—	—	V
	V_{OL}	I_{OL} = 1.6 mA	—	—	0.4	
Output leak current	I_{OZH}	V_{OUT} = 5.5 V	–2.0	—	2.0	µA
	I_{OZL}	V_{OUT} = 0 V	–2.0	—	2.0	
Input voltage	V_{IH}	—	4/5 V_{DD}	—	—	V
	V_{IL}	—	—	—	1/5 V_{DD}	
Input current	I_{IH}	V_{IN} = 5.5 V	–2.0	—	2.0	µA
	I_{IL}	V_{IN} = 0 V	–2.0	—	2.0	
Oscillation startup time	Ts	Ta = +25 °C	—	—	3.0	s

(2) AC Characteristics (GND=0 V , Ta = –30 °C ~ +70 °C)

Item	Symbol	Condition	V_{DD} = 5 V ± 10 %			Unit
			Min.	Typ.	Max.	
$\overline{SCK}$ frequency	f_{CLK}	—	—	—	500	kHz
$\overline{SCK}$ "L" time	t_{WCKL}	—	1.0	—	—	µs
$\overline{SCK}$ "H" time	t_{WCKH}	—	1.0	—	—	
$\overline{SCK}$ pause time	t_{PS}	—	1.0	—	—	
$\overline{CS0}$ setup time	t_{SCS}	—	0	—	—	
$\overline{CS0}$ hold time	t_{HCS}	—	0.5	—	—	
S_{IN} data setup time	t_{SD}	—	0.2	—	—	
S_{IN} data hold time	t_{HD}	—	0.2	—	—	
$\overline{WR}$ setup time	t_{SWR}	—	1.0	—	—	
$\overline{WR}$ hold time	t_{HWR}	—	0.5	—	—	
S_{OUT} delay time	$t_{DS}0$	CL=100 pF	—	150	500	ns
Time lag between $\overline{CS0}$, CS1 enable and S_{OUT} output	$t_{DSZ}1$	CL=100 pF	—	—	100	
Time lag between $\overline{CS0}$ disable and S_{OUT} high Z	$t_{DSZ}2$	CL=100 pF	—	—	100	
Time lag between CS1 enable and $\overline{TP_{OUT}}$ output	$t_{DPZ}1$	CL=100 pF	—	—	100	
Time lag between CS1 disable and $\overline{TP_{OUT}}$ high Z	$t_{DPZ}2$	CL=100 pF	—	—	100	

7.1.2. V_{DD} = 3 V

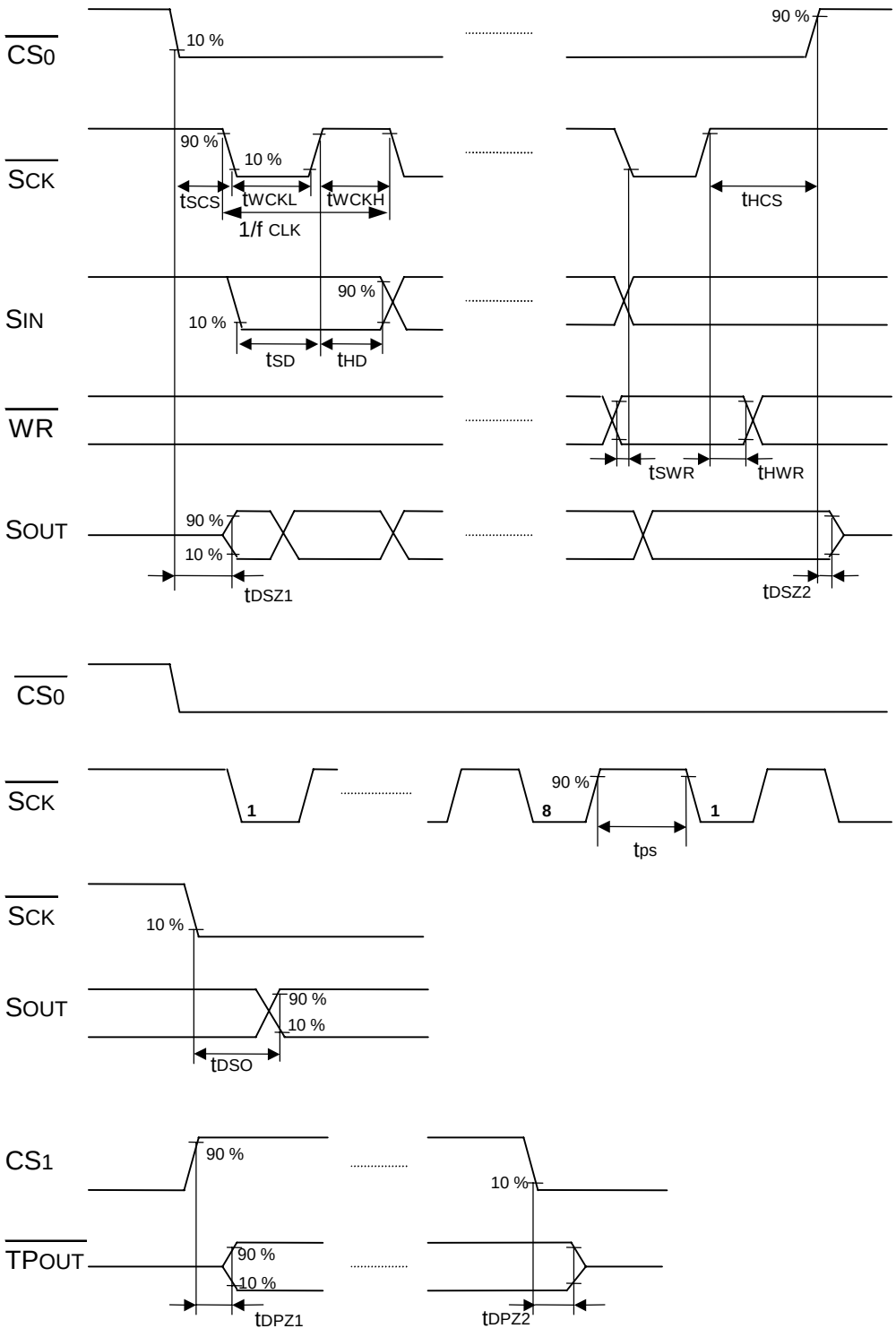
(1) DC Characteristics (GND=0 V , Ta = –30 °C ~ +70 °C)

Item	Symbol	Condition	V_{DD} = 3 V ±10 %			Unit
			Min.	Typ.	Max.	
Data retention voltage	V_{DH}	—	2.0	—	3.3	V
Current consumption	$I_{DD}1$ (normal operation)	$\overline{SCK}$ = 300 kHz $\overline{CS0}$ = L, CS1 = H	—	—	100	µA
	$I_{DD}2$ (backup operation)	$\overline{SCK}$ = 0 Hz $\overline{CS0}$ = H, CS1 = L	—	1.0	3.0	
Output voltage	V_{OH}	I_{OH} = –400 µA	V_{DD}–0.4	—	—	V
	V_{OL}	I_{OL} = 1.2 mA	—	—	0.4	
Output leak current	I_{OZH}	V_{OUT} = 3.3 V	–2.0	—	2.0	µA
	I_{OZL}	V_{OUT} = 0 V	–2.0	—	2.0	
Input voltage	V_{IH}	—	4/5 V_{DD}	—	—	V
	V_{IL}	—	—	—	1/5 V_{DD}	
Input current	I_{IH}	V_{IN} = 3.3 V	–2.0	—	2.0	µA
	I_{IL}	V_{IN} = 0 V	–2.0	—	2.0	
Oscillation startup time	T_S	Ta = +25 °C	—	—	3.0	s

(2) AC Characteristics (GND=0 V , Ta = –30 °C ~ +70 °C)

Item	Symbol	Condition	V_{DD} = 3 V ±10 %			Unit
			Min.	Typ.	Max.	
$\overline{SCK}$ frequency	f_{CLK}	—	—	—	300	kHz
$\overline{SCK}$ "L" time	t_{WCKL}	—	1.5	—	—	µs
$\overline{SCK}$ "H" time	t_{WCKH}	—	1.5	—	—	
$\overline{SCK}$ pause time	t_{PS}	—	1.5	—	—	
$\overline{CS0}$ setup time	t_{SCS}	—	0	—	—	
$\overline{CS0}$ hold time	t_{HCS}	—	1.0	—	—	
S_{IN} data setup time	t_{SD}	—	0.2	—	—	
S_{IN} data hold time	t_{HD}	—	0.2	—	—	
$\overline{WR}$ setup time	t_{SWR}	—	1.5	—	—	
$\overline{WR}$ hold time	t_{HWR}	—	1.0	—	—	
S_{OUT} delay time	t_{DSO}	CL=100 pF	—	300	500	ns
Time lag between $\overline{CS0}$, CS1 enable and S_{OUT} output	$t_{DSZ}1$	CL=100 pF	—	—	200	
Time lag between $\overline{CS0}$ disable and S_{OUT} high Z	$t_{DSZ}2$	CL=100 pF	—	—	200	
Time lag between CS1 enable and $\overline{TP_{OUT}}$ output	$t_{DPZ}1$	CL=100 pF	—	—	200	
Time lag between CS1 disable and $\overline{TP_{OUT}}$ high Z	$t_{DPZ}2$	CL=100 pF	—	—	200	

7.2. Timing Chart



8. How to use

8.1. Registers

8.1.1. Register Table

MODE 2 (User RAM register 2)								
Address					User RAM register			
	A3	A2	A1	A0	D3	D2	D1	D0
0	0	0	0	0	RA_{63}	RA_{62}	RA_{61}	RA_{60}

MODE 1 (User RAM register 1)								
Address					User RAM register			
	A3	A2	A1	A0	D3	D2	D1	D0
0	0	0	0	0	RA3	RA2	RA1	RA_0

MODE 0										
Address					Register designation	Counter control register				
	A3	A2	A1	A0		D3	D2	D1	D0	Register name
0	0	0	0	0	S1	S_8	S_4	S_2	S_1	1-second digit counter
1	0	0	0	1	S10	0	S_{40}	S_{20}	S_{10}	10-second digit counter
2	0	0	1	0	MI1	mi_8	mi_4	mi_2	mi_1	1-minute digit counter
3	0	0	1	1	MI10	0	mi_{40}	mi_{20}	mi_{10}	10-minute digit counter
4	0	1	0	0	H1	h_8	h_4	h_2	h_1	1-hour digit counter
5	0	1	0	1	H10	$\overline{PM}/AM$	0	h_{20}	h_{10}	10-hour digit counter
6	0	1	1	0	W	0	w_4	w_2	w_1	Day of the week digit counter
7	0	1	1	1	D1	d_8	d_4	d_2	d_1	1-day digit counter
8	1	0	0	0	D10	0	0	d_{20}	d_{10}	10-day digit counter
9	1	0	0	1	MO1	mo_8	mo_4	mo_2	mo_1	1-month digit counter
A	1	0	1	0	MO10	0	0	0	mo_{10}	10-month digit counter
B	1	0	1	1	Y1	y_8	y_4	y_2	y_1	1-year digit counter
C	1	1	0	0	Y10	y_{80}	y_{40}	y_{20}	y_{10}	10-year digit counter
D	1	1	0	1	CNT 1	TPS	30ADJ	CNTR	$24/\overline{12}$	Control register 1
E	1	1	1	0	CNT 2	BUSY	PONC	—	∗	Control register 2
F	1	1	1	1	CNT 3	SYSR	TEST	MS1	MS0	Control register 3

RA_4	RA_8
RA_{12}	RA_{16}
RA_{20}	RA_{24}
RA_{28}	RA_{32}
RA_{36}	RA_{40}
RA_{44}	RA_{48}
RA_{52}	RA_{56}
MS0	

RA_{64}	RA_{68}
RA_{72}	RA_{76}
RA_{80}	RA_{84}
RA_{88}	RA_{92}
RA_{96}	RA_{100}
RA_{104}	RA_{108}
RA_{112}	RA_{116}
MS0	

* In positive logic, "H" on the data bus corresponds to "1" in the register.
"ADDRESS_F" of MODE 1 and MODE 2 is the same as "ADDRESS_F" of MODE 0.

Notes
(1) Do not set invalid (out of range) data for the time and calendar. Otherwise counting errors may occur.
(2) At power-on (before initialization), the data for each bit are cleared. Write the registers to set the values.
(3) Always set the D0 bit (∗ bit) of the control register 2 to "0".
(4) When reading the D1 bit (— bit) of the control register 2, data of this bit are undefined.
(5) Always set the D3 bit (TEST bit) of the control register 3 to "0".

8.1.2. Register Bit Functions

<table>
<tr><th>Bit name</th><th>Function</th></tr>
<tr><td>Bit marked "0"</td><td>Unused bit that cannot be written. Always read as "0".</td></tr>
<tr><td>Second to year digit</td><td>BCD code. Data are written using increment method.</td></tr>
<tr><td>PM/ $\overline{\text{AM}}$</td><td>"1" indicates PM and "0" indicates AM. This bit can be read also when 24-hour format is selected (24/12=1). (AM: 00:00 to 11:59, PM: 12:00 to 23:59)</td></tr>
<tr><td>Day of the week digit</td><td>To be coded as 7-base counter.
Example
<table>
<tr><td>Data</td><td>0</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td></tr>
<tr><td>Coded day of the week</td><td>Sun.</td><td>Mon.</td><td>Tue.</td><td>Wed.</td><td>Thu.</td><td>Fri.</td><td>Sat.</td></tr>
</table></td></tr>
<tr><td>Year digit</td><td>Automatic leap year compensation up to 2099</td></tr>
<tr><td>User RAM area</td><td>30 × 4 bit SRAM</td></tr>
<tr><td>TPS
(Timing pulse selection)</td><td>Bit for selecting reference signal output waveform.

Note 1/10 Hz is not output for 10 seconds after power-on or system reset (output is "L").
<table>
<tr><th>TPS bit</th><th>Frequency (cycle time)</th></tr>
<tr><td>0</td><td>1024 Hz (976.5 µs)</td></tr>
<tr><td>1</td><td>1/10 Hz (10 s)</td></tr>
</table></td></tr>
<tr><td>30ADJ
(30 seconds adjustment)</td><td>Setting this bit to "1" performs 30 second adjustment.
The bit automatically resets when 30 second adjustment is completed (after 76.3 µs).</td></tr>
<tr><td>CNTR
(Counter reset)</td><td>Setting this bit to "1" resets the time and calendar counters.</td></tr>
<tr><td>24/ $\overline{\text{12}}$</td><td>24-hour or 12-hour format selection bit. When set to "1", 24-hour format is used. When set to "0", 12-hour format is used.</td></tr>
<tr><td>Busy</td><td>Used when reading/writing time and calendar counter data. Set to "1" when carry occurs.
<table>
<tr><th>BUSY bit</th><th>Mode</th><th>Meaning</th></tr>
<tr><td>0</td><td>No carry</td><td>Time/calendar counter read/write possible</td></tr>
<tr><td>1</td><td>Carry</td><td>Time/calendar counter read/write prohibited</td></tr>
</table></td></tr>
<tr><td>PONC
(Power-on-clear detection)</td><td>At power-on, the power-on-clear function automatically sets this bit to "1". This has the same effect as data initialization.
<table>
<tr><th>Register</th><th>Data</th></tr>
<tr><td>Time/calendar counters</td><td>00-year, 01-month, 01-day, AM 12-hour,
00-minute, 00- second, 0-day of the week</td></tr>
<tr><td>Control registers</td><td>All "0" (PONC = "1")</td></tr>
<tr><td>User RAM area</td><td>Undefined</td></tr>
</table>
When PONC is "1", data must be set. First clear this bit (this can be done by writing "1" to SYSR and then releasing system reset) and then set the time/calendar counters.</td></tr>
<tr><td>Bit marked " – "</td><td>Cannot be written. When read, the data are undefined.</td></tr>
<tr><td>Bit marked " ∗ "</td><td>Can be written but must always be set to "0".</td></tr>
<tr><td>SYSR
(System reset)</td><td>At SYSR = "1" all logic bits are initialized. The SYSR bit is reset to "0" by causing an up transition of CS0 and a down transition of SCK.
<table>
<tr><th>Register</th><th>Data</th></tr>
<tr><td>Time/calendar counters</td><td>00-year, 01-month, 01-day, AM 12-hour,
00-minute, 00- second, 0-day of the week</td></tr>
<tr><td>Control registers</td><td>All "0" (SYSR = "1")</td></tr>
<tr><td>User RAM area</td><td>Undefined</td></tr>
</table></td></tr>
<tr><td>TEST</td><td>Epson test bit. Must be set to "0".</td></tr>
<tr><td>MS0, MS1
(Mode selection)</td><td>These 2 bits serve for mode selection.
<table>
<tr><th>MS1</th><th>MS0</th><th>Mode name</th><th>Content</th></tr>
<tr><td>0</td><td>0</td><td>Mode 0</td><td>Time/calendar counters and control registers 1 - 3</td></tr>
<tr><td>0</td><td>1</td><td>Mode 0</td><td>Time/calendar counters and control registers 1 - 3</td></tr>
<tr><td>1</td><td>0</td><td>Mode 1</td><td>User RAM area (RA_0 - RA_{59}) and control register 3</td></tr>
<tr><td>1</td><td>1</td><td>Mode 2</td><td>User RAM area (RA_{60} - RA_{119}) and control register 3</td></tr>
</table></td></tr>
</table>

8.2. Register Description

8.2.1. Time/Calendar Counter Registers

· In normal mode (CNTR = "0"), the counter is incremented by a write operation.

(1) Second digit counter

Counts values from 0 to 59. The counter can be read and incremented. When the second digit counter is incremented, fractions below full seconds are reset. Therefore a carry occurs 1 second after the increment operation is finished.

A3	A2	A1	A0	Name	D3	D2	D1	D0	Register contents
0	0	0	0	S1	S_8	S_4	S_2	S_1	1-second digit counter
0	0	0	1	S10	0	S_{40}	S_{20}	S_{10}	10-second digit counter

(2) Minute digit counter

A3	A2	A1	A0	Name	D3	D2	D1	D0	Register contents
0	0	1	0	MI1	mi_8	mi_4	mi_2	mi_1	1-minute digit counter
0	0	1	1	MI10	0	mi_{40}	mi_{20}	mi_{10}	10-minute digit counter

Counts values from 0 to 59. The counter can be read and incremented.

(3) Hour digit counter

A3	A2	A1	A0	Name	D3	D2	D1	D0	Register contents
0	1	0	0	H1	h_8	h_4	h_2	h_1	1-minute digit counter
0	1	0	1	H10	PM/AM	0	h_{20}	h_{10}	10-minute digit counter

Counts values from 0 to 23. The counter can be read, and the 1-hour digit counter can be incremented. (The 10-hour digit counter cannot be incremented.)

D0 in the control register 1 sets the 12-hour/24-hour display format.

24/12 bit	Displayed time
0 (12-hour format)	AM 12:00 to AM 11:59, PM 12:00 to PM 11:59
1 (24-hour format)	AM 00:00 to AM 11:59, PM 12:00 to PM 23:59

* PM/AM bit: This bit is output also when 24-hour format is selected.
* Time keeping is not affected also when the 12-hour/24- hour format is switched during clock operation.

(4) Day of the week digit counter

A3	A2	A1	A0	Name	D3	D2	D1	D0	Register contents
0	1	1	0	W	0	w_4	w_2	w_1	Day of the week digit counter

Counts values from 0 to 6. The counter can be read and incremented. The correspondence between count value and day of the week is set by the user.

Example

Data	0	1	2	3	4	5	6
Coded day of the week	Sun.	Mon.	Tue.	Wed.	Thu.	Fri.	Sat.

(5) Day digit counter

A3	A2	A1	A0	Name	D3	D2	D1	D0	Register contents
0	1	1	1	D1	d_8	d_4	d_2	d_1	1-day digit counter
1	0	0	0	D10	0	0	d_{20}	d_{10}	10-day digit counter

The counter value is different depending on the month.

(a) For long months (1, 3, 5, 7, 8, 10, 12), the counter counts values from 1 to 31. The counter can be read and incremented.
(b) For short months (4, 6, 9, 11), the counter counts values from 1 to 30. The counter can be read and incremented.
(c) For February, the counter counts values from 1 to 29 if it is a leap year and from 1 to 28 in other years. The counter can be read and incremented.

(6) Month digit counter

A3	A2	A1	A0	Name	D3	D2	D1	D0	Register contents
1	0	0	1	MO1	mo_8	mo_4	mo_2	mo_1	1-month digit counter
1	0	1	0	MO10	0	0	0	mo_{10}	10-month digit counter

Counts values from 1 to 12. The counter can be read and incremented.

(7) Year digit counter

A3	A2	A1	A0	Name	D3	D2	D1	D0	Register contents
1	0	1	1	Y1	y_8	y_4	y_2	y_1	1-year digit counter
1	1	0	0	Y10	y_{80}	y_{40}	y_{20}	y_{10}	10-year digit counter

Counts values from 0 to 99 for the last two digits of the year. The counter can be read and incremented. Until 2099, leap year compensation is automatically provided. ('92, '96, '00, '04, '08, '12, '16, '20 ... are leap years.)

8.2.2. Control Registers

(1) Control register 1

A3	A2	A1	A0	Name	D3	D2	D1	D0	Register contents
1	1	0	1	CNT 1	TPS	30ADJ	CNTR	24/12	Control register 1

Control register 1 performs 12-hour/24-hour display format switching, digit counter reset, 30 second adjustment, and timing pulse signal switching. The register allows data read and write.

(a) TPS bit (D3)

The TPS bit selects the timing pulse output waveform.

TPS bit	Frequency (cycle)	"L" level duty
0	1024 Hz (976.5 μs)	1/2 (488.28 μs)
1	1/10 Hz (10 s)	3/5 (6 s)

1/10 Hz is not output for 10 seconds after power-on or system reset (output is "L").

(b) 30ADJ bit (D2)

When "1" is written to this bit, one of the following reset operations is carried out.

Seconds digit before adjustment	Seconds digit after adjustment
29 seconds or less	Seconds reset to "00" without carry to 1-minute digit
30 seconds or more	Seconds reset to "00" with carry to 1-minute digit

When "1" was written to the 30ADJ bit, the bit automatically resets itself to "0" within 76.3 μs The 30 second adjustment function also resets fractions below full seconds. The $\overline{\text{TPOUT}}$ 1/10 Hz duty changes for one cycle only during 30 second adjustment.

(c) CNTR bit (D1)

The CNTR bit resets the time/calendar counters.

CNTR bit	Content
0	Normal mode (time/calendar counters can be incremented)
1	Selected counter is reset to "0"

* For counters other than the year, selecting either the 1 or the 10 digit counter will reset both counters.

When CNTR is used to reset the seconds, fractions below full seconds are also reset. The $\overline{\text{TPOUT}}$ 1/10 Hz duty changes for one cycle only during reset.

(d) 24/12 bit (D0)

The 24/12 bit serves to switch between 12-hour and 24-hour format.

24/12 bit	Displayed time
0 (12-hour format)	AM 12:00 to AM 11:59, PM 12:00 to PM 11:59
1 (24-hour format)	AM 00:00 to AM 11:59, PM 12:00 to PM 23:59

* PM/AM bit: This bit is output also when 24-hour format is selected.
* Time keeping is not affected also when the 12-hour/24- hour format is switched during clock operation.

(2) Control register 2

A3	A2	A1	A0	Name	D3	D2	D1	D0	Register contents
1	1	1	0	CNT 2	BUSY	PONC	—	*	Control register 2

Control register 2 provides flags for carry detect and power-on-clear detect.

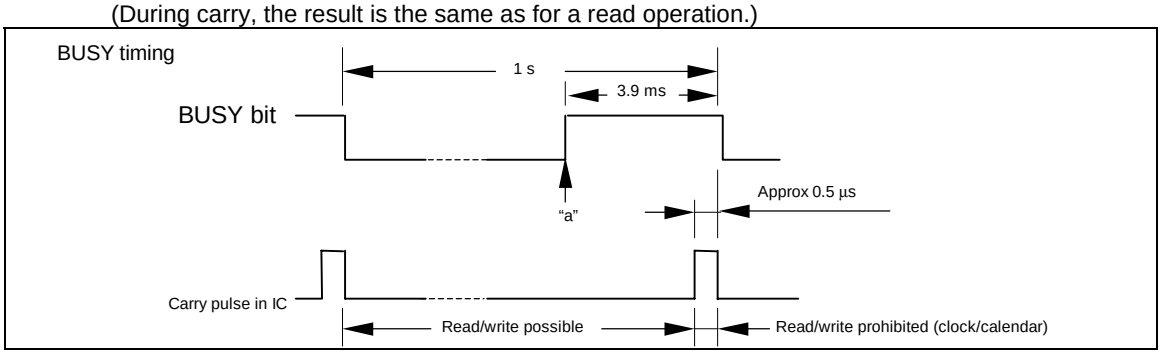
(a) BUSY bit (D3)

The BUSY bit serves for time/calendar counter digit carry detection.

BUSY bit	Mode	Meaning
0	Normal mode	Time/calendar counter read/write possible
1	Carry	Time/calendar counter read/write prohibited

If the BUSY bit is "L", carry does not occur for at least 3.9 ms. (Also when read/write is carried out at point "a" in the chart below, carry does not occur for 3.9 ms.)
Take the processing time into consideration and design the read/write operation to complete within 3.8 ms.
Clock read/write during carry

· Read It may not be possible to read correct data.
· Write Because the clock has priority, the write operation does not increment the counter.
(During carry, the result is the same as for a read operation.)



(b) PONC bit (D2)

The PONC bit is the power-on-clear detection bit (see next page). It is set to "1" when power-on-clear is detected. The PONC bit is reset (1 → 0) by setting the SYSR bit to "1".

(c) D1 bit (bit marked "—")

When this bit is read, data are undefined.

(d) D0 bit (bit marked " * ")

When writing this bit, always set it to "0".

(3) Control register 3

Control registers 3 serves for reading and writing data for address mode switching and making system reset settings.
The control register 3 applies to modes 0 - 2.

A3	A2	A1	A0	Name	D3	D2	D1	D0	Register contents
1	1	1	1	CNT 3	SYSR	TEST	MS_1	MS_0	Control register 3

(a) SYSR bit (D3)

The SYSR bit serves for clearing all counter registers (see section on initialization on next page).
This bit is reset by making $\overline{CS0}$ High and $\overline{SCK}$ Low.

(b) TEST bit (D2)

The TEST bit serves to switch the IC to the test mode.
Note Be sure to permanently set this bit to "0". Otherwise correct operation is not assured.

(c) MS1, MS0 bit (D1, D0)

The MS1 and MS0 bits serve for address switching.

MS1	MS0	Mode name	Content
0	0	MODE 0	Time/calendar counters and control registers 1 - 3
0	1	MODE 0	Time/calendar counters and control registers 1 - 3
1	0	MODE 1	User RAM area (RA_0 - RA_{59}) and control register 3
1	1	MODE 2	User RAM area (RA_{60} - RA_{119}) and control register 3

8.3. How to use

8.3.1. Data Read

When $\overline{CS0}$ is "L", the serial address data input at SIN is read at the leading edge of $\overline{SCK}$. Next, when $\overline{WR}$ = "H" is taken in on the 8th pulse leading edge of $\overline{SCK}$ the counter control register or RAM address is selected. The data of the selected counter control register or RAM address are output in the following cycle from SOUT, in sync with the $\overline{SCK}$ trailing edge.

8.3.2. Data Write/Modify

When $\overline{CS0}$ is "L", the serial address data input at SIN is read at the leading edge of $\overline{SCK}$. Next, when $\overline{WR}$ = "H" is taken in on the 8th pulse leading edge of $\overline{SCK}$, the counter control register or RAM address is selected, and data are written as shown below.

Item	Content
Time/calendar	Counter, counter data increment (+1) *
Control register/RAM	Serial address/lower 4 bit of data are written

The selected counter register or RAM address data are output in the following cycle from SOUT, in sync with the $\overline{SCK}$ trailing edge.

* The hour digit counter can be incremented via the 1-hour digit counter.

8.3.3. Initialize

(1) System reset

When the SYSR bit in the control register 3 is set to "1", all logic bits are initialized. The SYSR bit is reset to "0" by causing an up transition of $\overline{CS0}$ and a down transition of $\overline{SCK}$.

Register	Data
Time/calendar counters	- year, 01-month, 01-day, AM 12-hour, 00-minute, 00- second, 0-day of the week
Control registers	All "0" (SYSR = "1")
User RAM area	Undefined

Until system reset is released, $\overline{TPOUT}$ is fixed to "L".

1/10 Hz is not output for 10 seconds after system reset is released.

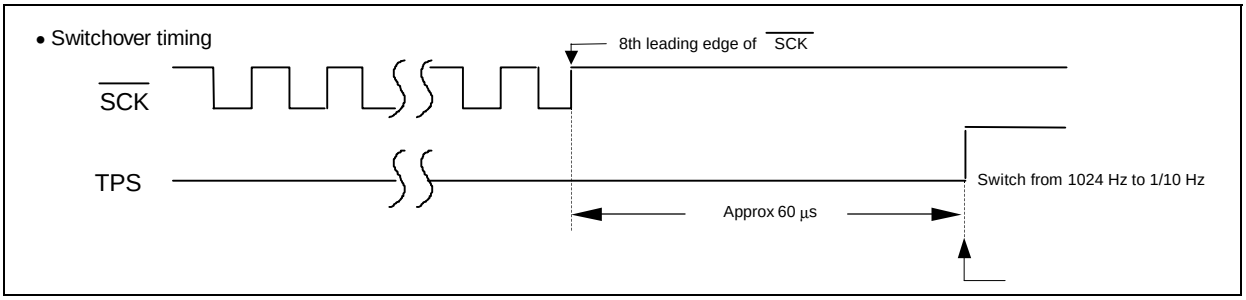
(2) Power-on-clear

At power-on, the power-on-clear function automatically performs a sequence identical to system reset. However, because the PONC bit remains at "1", a system reset must be performed to set the PONC bit to "0" before setting the time and calendar.

8.3.4. Timing Pulse Output

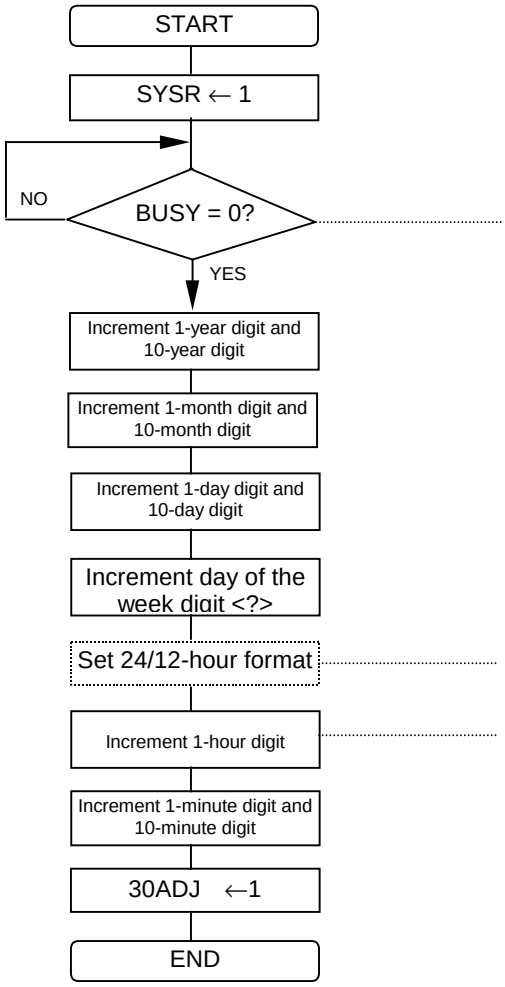
The timing pulse is output from the $\overline{TPOUT}$ pin.

Normally, a 1024 Hz signal is output. By setting the TPS bit in the control register 1 to "1", this can be switched to 1/10 Hz.



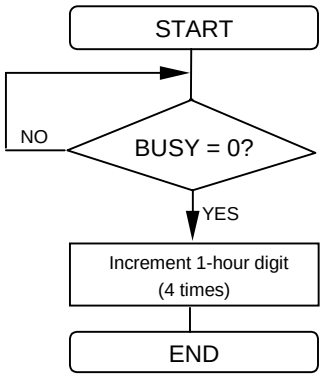
8.3.5. Sample Operation Flow Charts

(1) Time/calendar initialize example
(Example for initialization through power-on-clear when battery was changed etc.)



- Release PONC bit = "1" (1 → 0)
- While BUSY = "1", a carry operation is in progress and the setting should not be carried out. The following processing steps must be completed within 996 ms after SYSR ← "1" or after the BUSY bit down transition was detected. If the process takes longer, the BUSY bit must be checked again for continued processing.
- It is advisable to start the setting from the year digit, to prevent setting nonexistent data.
- When the 1-digit of the year, month, day, hour, minute, or second is set, carry to the 10-digit can occur.
- It is advisable to set this before setting the hour digit, to prevent setting nonexistent data.
- Set the 10-hour digit by incrementing the 1-hour digit.

(2) Time/calendar modify example (8:00 → 12:00)

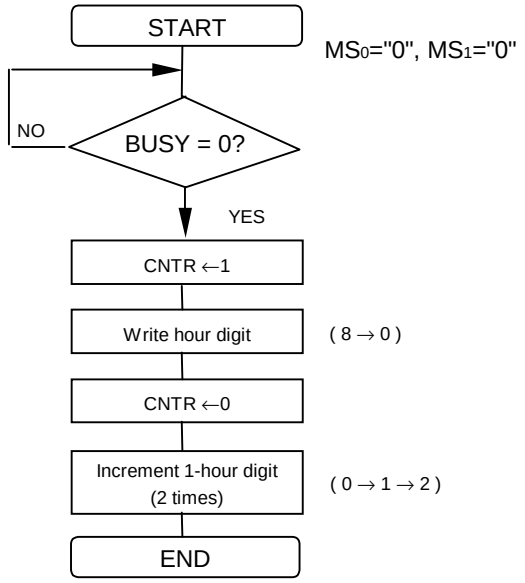


MS0=0, MS1=0

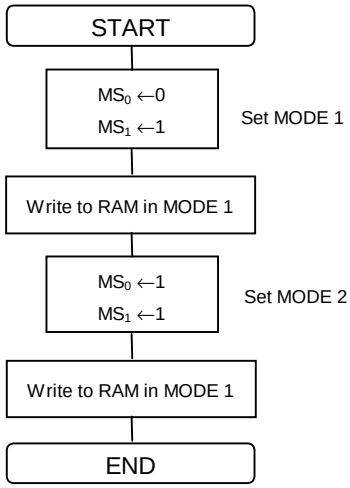
While BUSY = "1", a carry operation is in progress and the setting should not be carried out.

4 times (8 → 9 → 10→ 11→ 12)
↑
10-hour digit is automatically carried.
The processing should be completed within 3.8 ms after detecting BUSY = "0".

(3) Time/calendar modify example using counter reset (8:00 → 2:00)



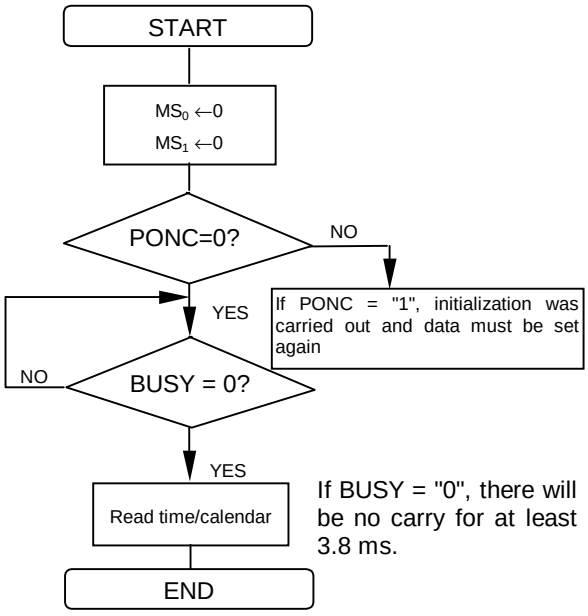
(4) RAM write example



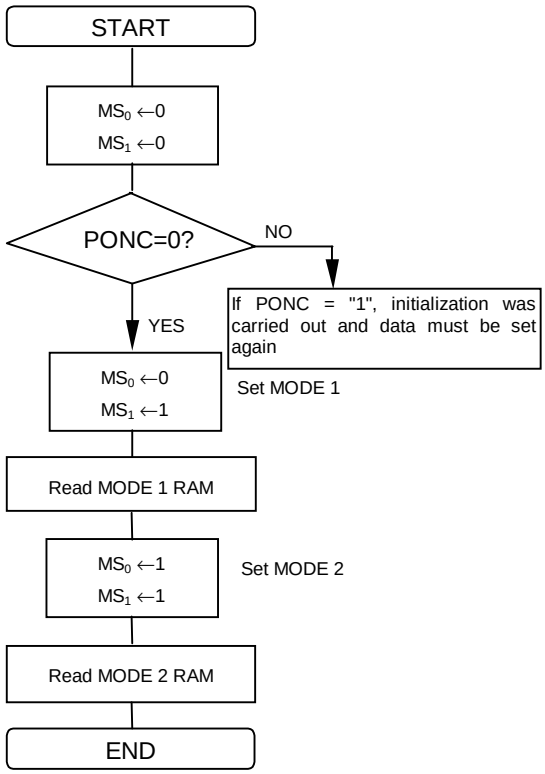
Note 1 If processing is not completed within 3.8 ms, check the BUSY bit again.

Note 2 Reset (CNTR ← "1") applies to the digits for which writing was performed [1-hour digit and 10-hour digit in example (3)]. Consequently, to change the setting from 11:00 to 2:00, the hour digit must be reset (CNTR → "1").
For the year, CNTR is used separately for the 1-year digit and 10-year digit. Performing CNTR on the 1-year digit does not change the 10-year digit. Conversely, performing CNTR on the 10-year digit does not change the 1-year digit.

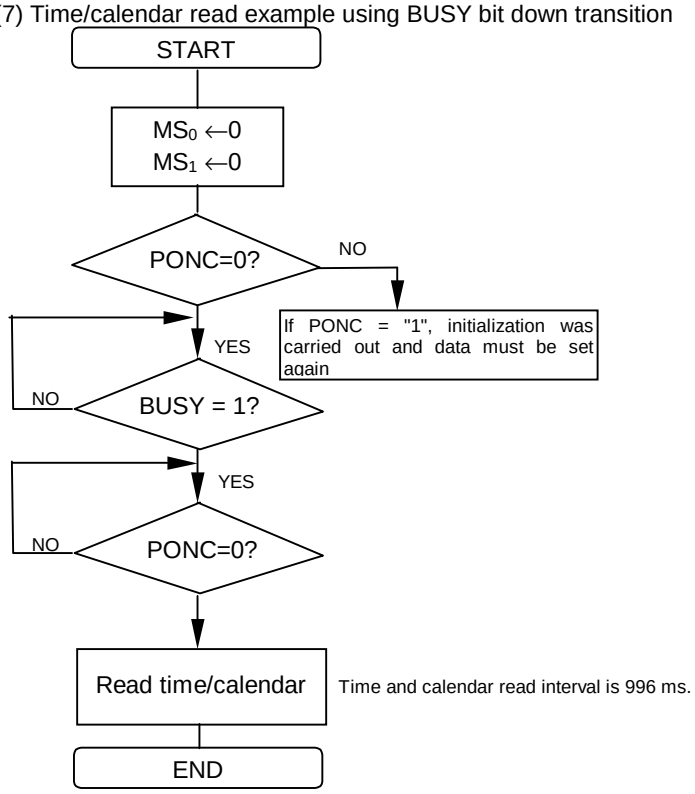
(5) Time/calendar read example



(6) RAM read example

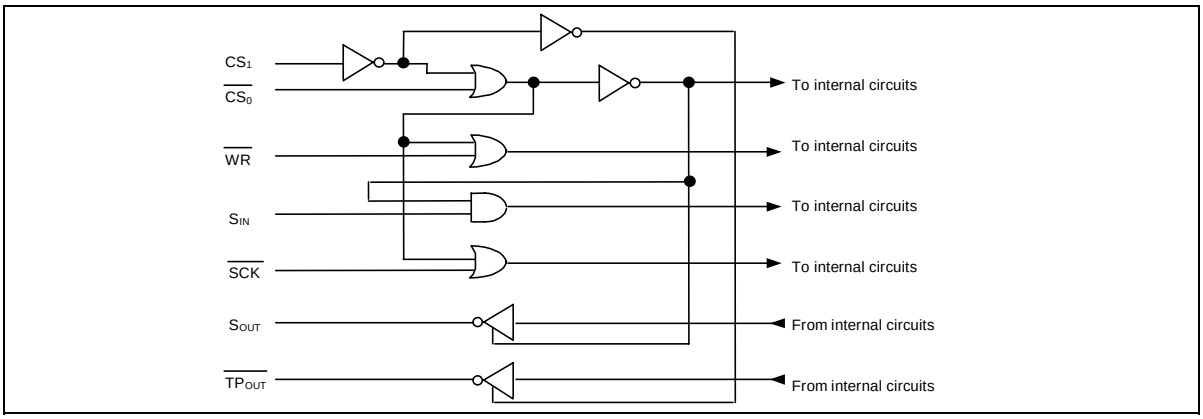


(7) Time/calendar read example using BUSY bit down transition



8.3.6. CS1 and $\overline{CS0}$ Operation

When designing a floating arrangement, take the following into consideration. $\overline{CS0}$ can be floating while CS1 = "L", but CS1 can never be floating. (Otherwise a through current would flow, leading to increased current consumption during operation on backup battery power.) When CS1 = "L", input is disabled, and SOUT and $\overline{TPOUT}$ are at high impedance.

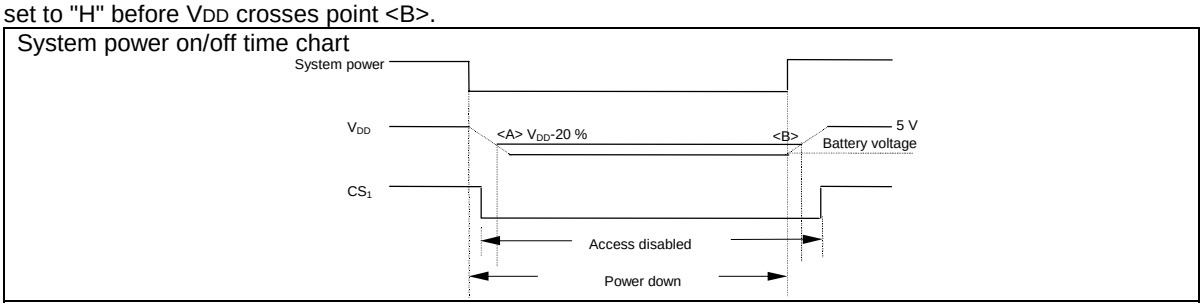


8.3.7. System Power Down During Interface Operation

When the system power goes down during interface operation with the CPU, causing CS1 to become "L", the incomplete data will be invalid. Immediately after system power restoration, when CS1 has become "H", the output data from SOUT are undefined for one cycle.

8.3.8. Power Supply and CS1 Operation

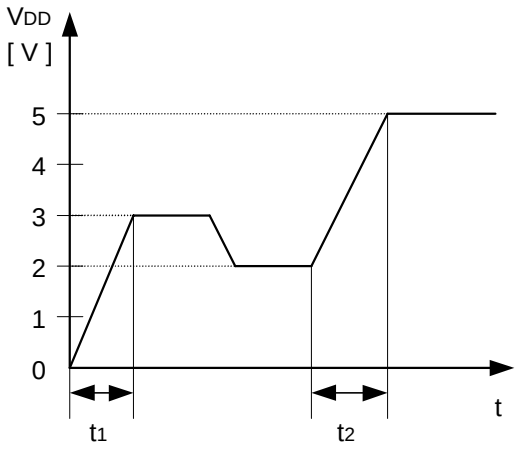
When the system power is shut down, VDD falls to the battery voltage. When used at VDD ±10%, CS1 must be set to "L" before VDD crosses point <A> in the diagram below. When system power is restored, CS1 must be set to "H" before VDD crosses point <B>.



8.3.9. Power-On Reset

When the system power is turned on, the power-on reset function operates automatically, performing a sequence identical to system reset. However, because the PONC bit remains at "1", a system reset must be performed to set the PONC bit to "0" before setting the time and calendar.

The conditions for power-on reset and the conditions for data retention and normal IC operation during power fluctuation are shown below.



t1: Condition for power-on reset

t2: Condition for data retention and normal IC operation during power-on

Note: 3 V and 5 V are recommended voltages. 2 V is the backup voltage.

Ta = –30 °C to +70 °C

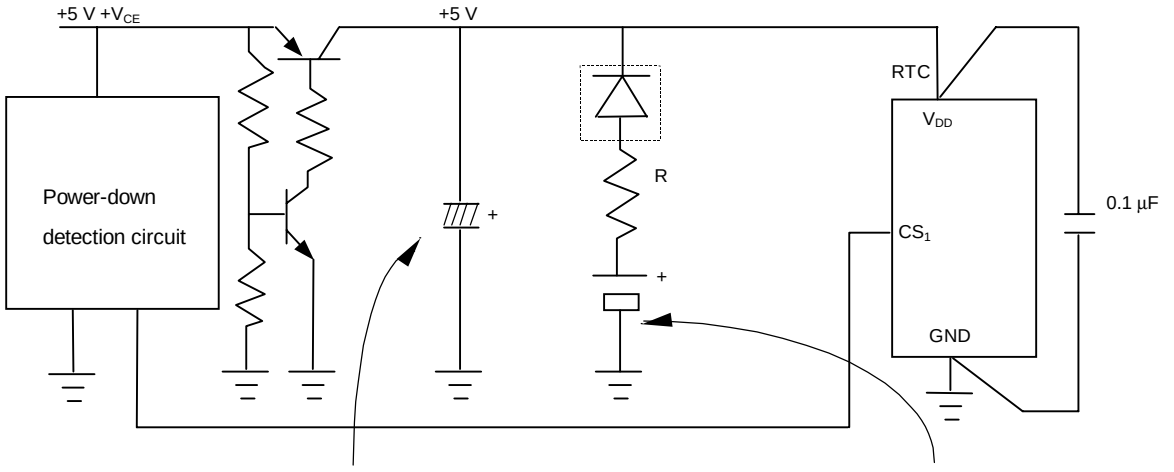
t 1	Condition tR for power-on reset at $0^{+0.3}$ V → 3 V or $0^{+0.3}$ V → 5 V (Note 1)	1.0 µs/V ≤ tR ≤ 1.6 ms/V
t 2	Condition tR for no power-on reset at 2 V → 3 V or 2 V → 5 V (Note 2)	1.0 µs/V ≤ tR ≤ 1.6 ms/V

Note 1 The voltage level before initial power-on should be 0.3 V or less. If powering up from an intermediate potential, power-on reset may not be performed correctly. Be sure to verify correct operation.

Note 2 Within the voltage range for data retention and clock operation (2.0 V - 5.5 V), power-on reset is designed not to be performed under the above conditions, to prevent data loss. When the voltage level falls below 2 V, operation and data retention are no longer assured.

Note 3 During power-on or power restoration from an intermediate potential outside of the assured operation range (0.3 V - 1.9 V), the power-on reset circuit will not operate normally, leading to possible malfunction. If the backup battery voltage has fallen below 2.0 V, the VDD pin of the RTC must be temporarily set to ground potential before restoring the power.

8.3.10. Power Supply Connection Example



Use a high capacitance value here to guard against reverse current flowing from the collector to the emitter of the transistor during transition from power on to power off.

Secondary battery or lithium battery. (Lithium battery requires the diode shown in ⋯. Regarding the value of the resistor R, consult the battery manufacturer.

8.3.11. Processing of Non-Existent Data

(1) If the month digit is incremented while the current setting is January 31, a non-existent setting will result (February 31). Carry from the hour digit will cause this setting to become March 1.

	Month digit incremented		Carry from hour digit	
Jan. 31	→	Feb. 31	→	Mar. 01

(2) If the year digit is incremented while the current setting is February 29 of a leap year, a non-existent setting will result (February 29 of a non-leap year). Carry from the hour digit will cause this setting to become March 1.

	Year digit incremented		Carry from hour digit	
Feb. 29 00	→	Feb. 29 01	→	Mar. 01 01

When the following non-existent data are set (February 30), incrementing the 10-day digit causes an overflow in the 10-day digit, clearing the 1-day digit.

	10-day digit incremented once		10-day digit incremented once	
Feb. 30	→	Feb. 00	→	Feb. 10
Feb. 29	→	Feb. 01		

When a valid date is set, overflow of the 10-day digit does not clear the 1-day digit.

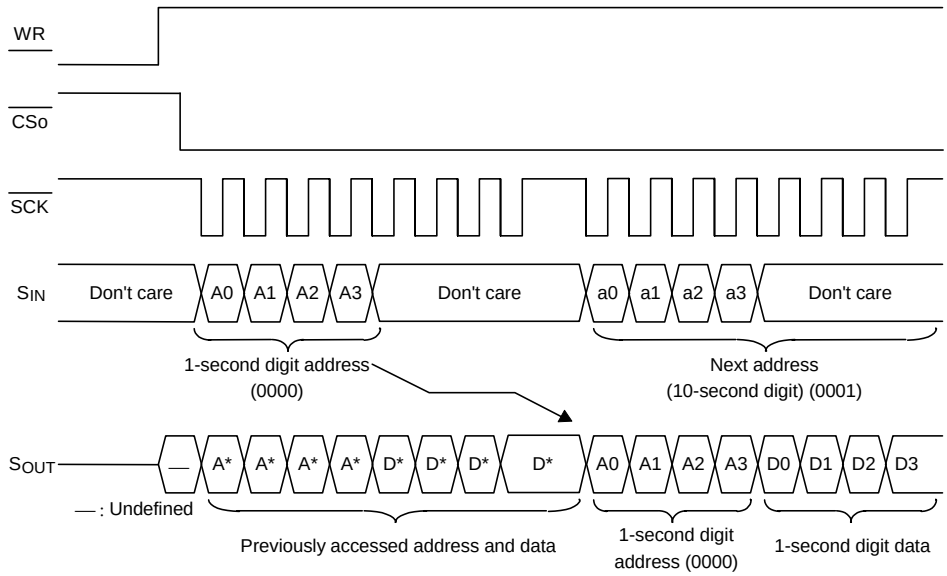
(3) When the 10-day digit is incremented past "31", the day digit counter becomes "01".

(4) When the 10-month digit is incremented, the month digit overflow processing will differ according to the month.

		10-month digit incremented once			
Non-existent month	00 month	→	Oct.		
	Oct.	→	00 month	Non-existent month	
	Nov.	→	Jan.		
	Dec.	→	Feb.		
	Mar. - Sep.	→	Jan.		

8.3.12. Timing Charts

(1) Data readout example



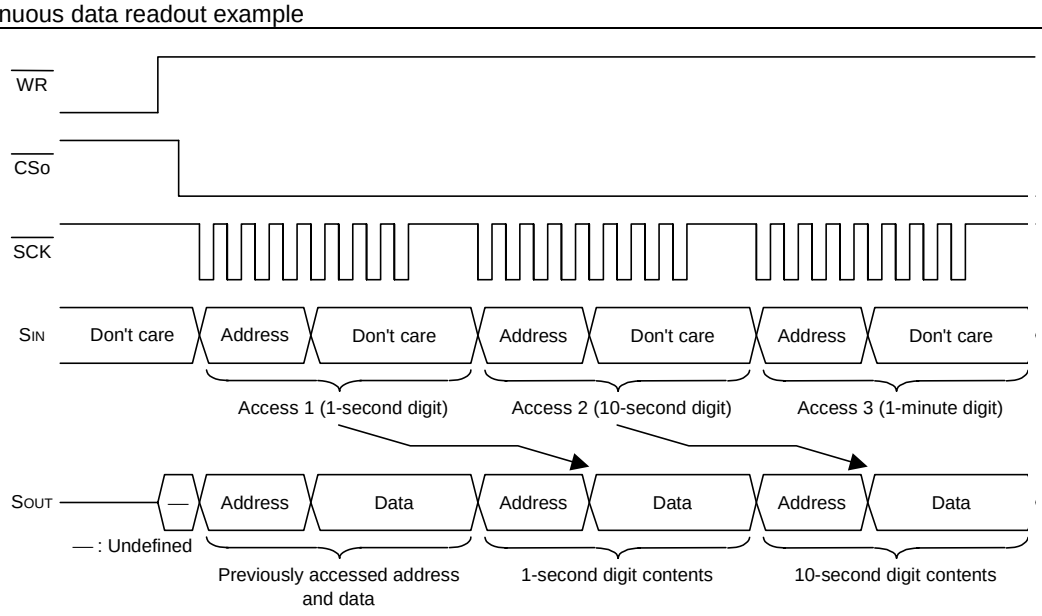
· When specifying the next data read access, the previously accessed address and data appear at SOUT.

· Same applies for reading from SRAM.

SIN : Input at leading edge of $\overline{SCK}$

SOUT : Output at trailing edge of $\overline{SCK}$

(2) Continuous data readout example



· When specifying the next data read access, the previously accessed address and data appear at SOUT.

SIN : Input at leading edge of $\overline{SCK}$

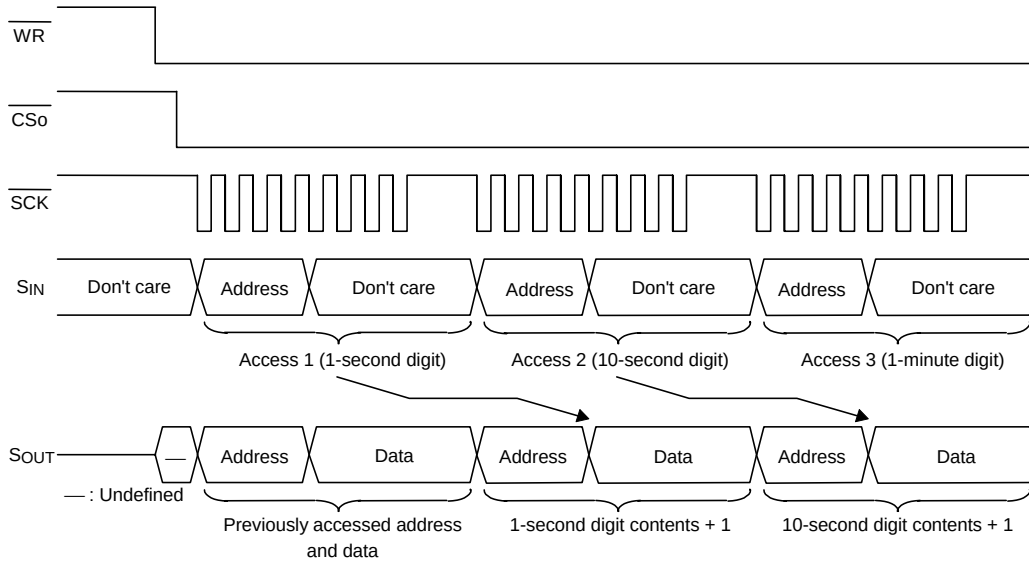
SOUT : Output at trailing edge of $\overline{SCK}$

Additional information

· When $\overline{CS0}$ is "L", the serial address data input at SIN are read at the leading edge of $\overline{SCK}$. Next, when WR = "H" is taken in on the 8th pulse leading edge of $\overline{SCK}$, the counter control register or RAM address is selected, and the data from the selected counter control register or RAM address are output from SOUT in sync with the trailing edge of $\overline{SCK}$.

· When the $\overline{SCK}$ clock is less than 8 pulses, the module enters the command standby mode. When the $\overline{SCK}$ clock is more than 8 pulses, the command is not input correctly. The internal $\overline{SCK}$ clock counter is cleared at the leading edge of $\overline{CS0}$.

(3) Time/calendar continuous write example (CNTR=0)



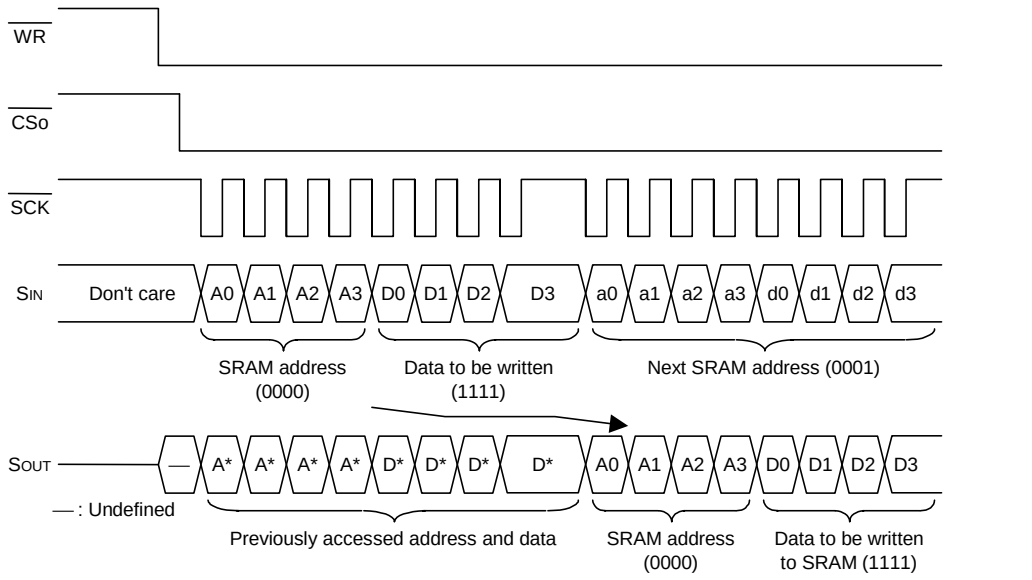
· The write result appears at SOUT when specifying the next access. When wanting to check the write result, it is therefore necessary to specify another read or write operation. (When using write access, note that the data of that address will be further incremented by 1.)

· For continuous write operations, the $\overline{CS0}$ must be kept "L" for the required number of increments (+1).

SIN : Input at leading edge of $\overline{SCK}$

SOUT : Output at trailing edge of $\overline{SCK}$

(4) SRAM data write example



· The write result appears at SOUT when specifying the next access. When wanting to check the write result, it is therefore necessary to specify another read or write operation.

· SIN data are valid only during SRAM write access.

SIN : Input at leading edge of $\overline{SCK}$

SOUT : Output at trailing edge of $\overline{SCK}$

Additional information

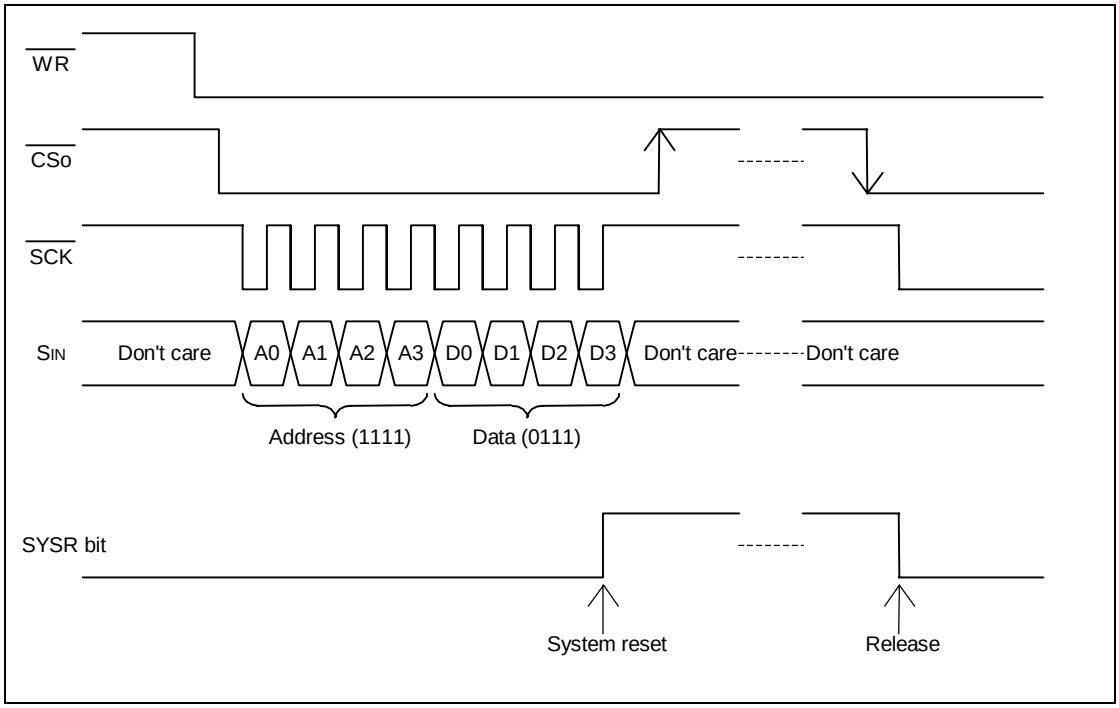
When $\overline{CS0}$ is "L", the serial address data input at $\overline{SIN}$ are read at the leading edge of $\overline{SCK}$. Next, when $\overline{WR}$ = "H" is taken in on the 8th pulse leading edge of $\overline{SCK}$., the counter control register or RAM address is selected, and data are written as shown below.

<table>
<tr><td>Time/calendar (CNTR = "0")</td><td>Counter data are incremented.
Example
<table>
<tr><th>Data before incrementing</th><th>Number of incrementing steps</th><th>Data after incrementing</th></tr>
<tr><td>0</td><td>4</td><td>4</td></tr>
<tr><td>8</td><td>3</td><td>11 (10-digit is carried automatically.)</td></tr>
</table></td></tr>
<tr><td>Control register and SRAM</td><td>Address and 4-bit data are written.</td></tr>
</table>

The selected counter register or RAM address data are output in the following cycle from SOUT, in sync with the $\overline{SCK}$ trailing edge.

(5) System reset

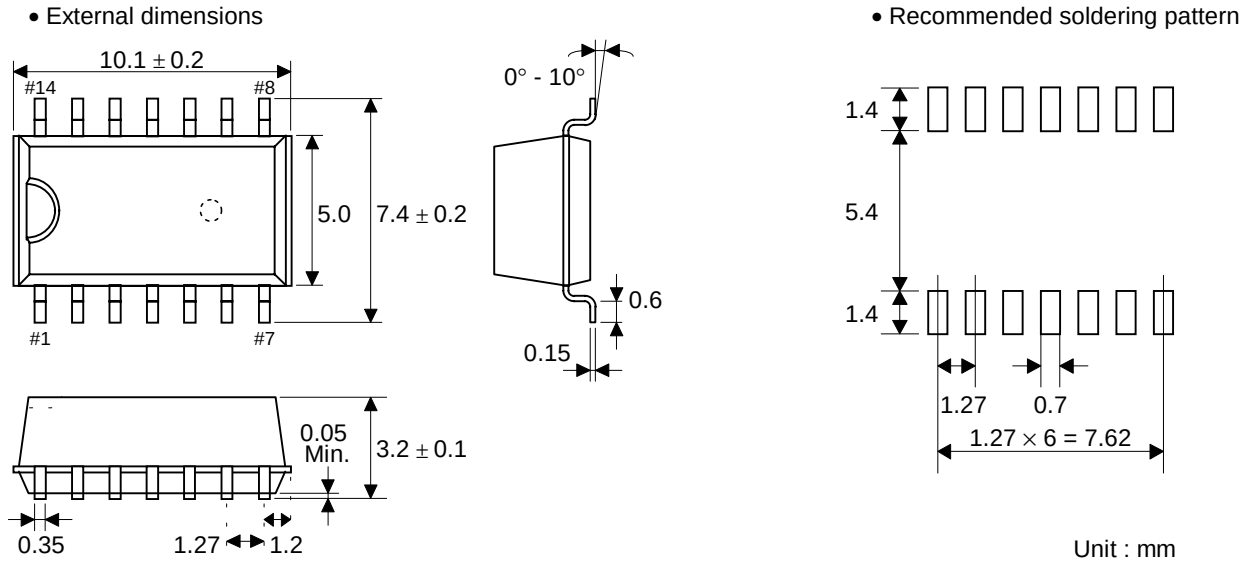
The SYSR (system reset) condition can be released by causing an up transition of $\overline{CS0}$ and a down transition of $\overline{SCK}$.



9. External dimensions / Marking layout

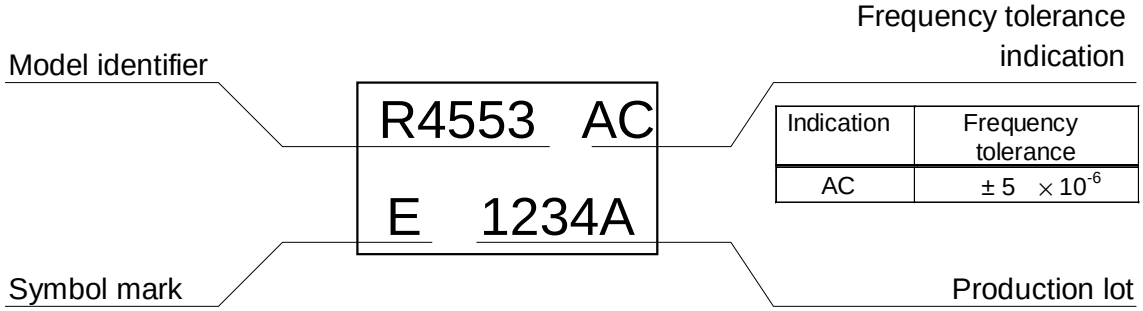
9.1. External dimensions

RTC - 4553 (SOP-14pin)



9.2. Marking layout

RTC – 4553AC (SOP-14pin)

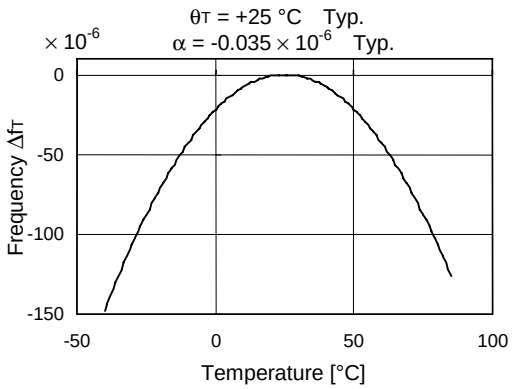


Indication	Frequency tolerance
AC	± 5 × 10^{-6}

∗ Contents displayed indicate the general markings and display, but are not the standards for the fonts, sizes and positioning.

10. Reference Data

(1) Frequency/temperature characteristics



[Calculating the frequency stability]

1. Frequency/temperature characteristics are approximated according to the following equation.

$\Delta f_T = \alpha\ (\theta_T - \theta_X)^2$

Δf_T		: Frequency tolerance at given temperature
α	($1 / °C^2$)	: Secondary temperature coefficient ($(-0.035 \pm 0.005) \times 10^{-6} / °C^2$)
θ_T	(°C)	: Peak temperature (+25°C ± 5°C)
θ_X	(°C)	: Given temperature

2. To calculate the clock accuracy, add the frequency tolerance and voltage characteristics

$\Delta f/f = \Delta f/fo + \Delta f_T + \Delta f_V$

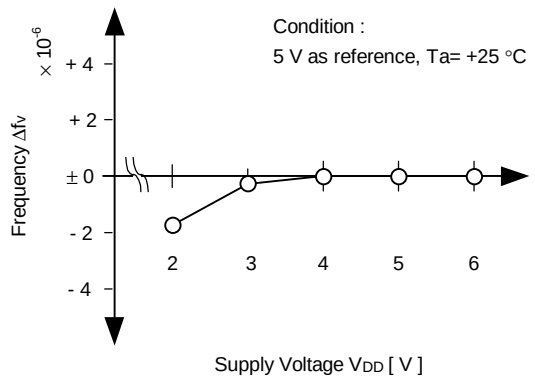
$\Delta f/f$	: Clock accuracy at given temperature and voltage (frequency stability)
$\Delta f/fo$	: Frequency tolerance
Δf_T	: Frequency deviation at given temperature
Δf_V	: Frequency deviation at given voltage

3. Calculating the daily deviation

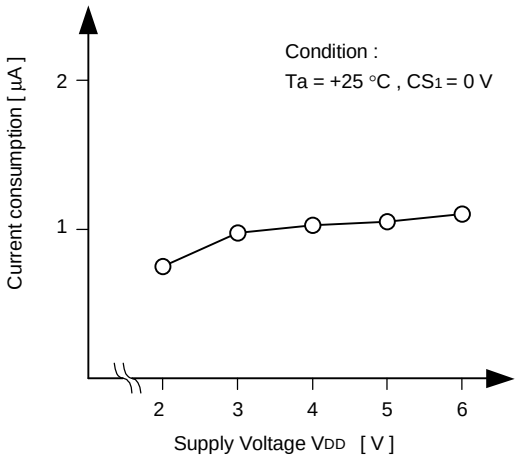
Daily deviation = $\Delta f/f$ ´ 86400 (seconds)

* For example, at $\Delta f/f = 11.574 ´ 10^{-6}$, the deviation is about 1 second per day.

(2) Frequency/voltage characteristics example



(3) Current consumption/voltage characteristics example



Note These data are reference values for the sample lot.

11. Application notes

11.1. Notes on handling

This module uses a C-MOS IC to realize low power consumption. Carefully note the following cautions when handling.

(1) Static electricity

While this module has built-in circuitry designed to protect it against electrostatic discharge, the chip could still be damaged by a large discharge of static electricity. Containers used for packing and transport should be constructed of conductive materials. In addition, only soldering irons, measurement circuits, and other such devices which do not leak high voltage should be used with this module, which should also be grounded when such devices are being used.

(2) Noise

If a signal with excessive external noise is applied to the power supply or input pins, the device may malfunction or "latch up." In order to ensure stable operation, connect a filter capacitor (preferably ceramic) of greater that 0.1 μF as close as possible to the power supply pins (between V_{DD} and GND). Also, avoid placing any device that generates high level of electronic noise near this module.

∗ Do not connect signal lines to the shaded area in the figure shown in Fig.1 and, if possible, embed this area in a GND land.

(3) Voltage levels of input pins

When the input pins are at the mid-level, this will cause increased current consumption and a reduced noise margin, and can impair the functioning of the device. Therefore, try as much as possible to apply the voltage level close to V_{DD} or GND.

(4) Handling of unused pins

Since the input impedance of the input pins is extremely high, operating the device with these pins in the open circuit state can lead to unstable voltage level and malfunctions due to noise. Therefore, pull-up or pull-down resistors should be provided for all unused input pins. (except L1–L5 pins)

11.2. Notes on packaging

(1) Soldering temperature conditions

If the temperature within the package exceeds +260 °C, the characteristics of the crystal oscillator will be degraded and it may be damaged. Therefore, always check the mounting temperature before mounting this device. Also, check again if the mounting conditions are later changed.

∗ See Fig.2 for the soldering conditions of SMD products.

(2) Mounting equipment

While this module can be used with general-purpose mounting equipment, the internal crystal oscillator may be damaged in some circumstances, depending on the equipment and conditions. Therefore, be sure to check this. In addition, if the mounting conditions are later changed, the same check should be performed again.

(3) Ultrasonic cleaning

Depending on the usage conditions, there is a possibility that the crystal oscillator will be damaged by resonance during ultrasonic cleaning. Since the conditions under which ultrasonic cleaning is carried out (the type of cleaner, power level, time, state of the inside of the cleaning vessel, etc.) vary widely, this device is not warranted against damage during ultrasonic cleaning.

(4) Mounting orientation

This device can be damaged if it is mounted in the wrong orientation. Always confirm the orientation of the device before mounting.

(5) Leakage between pins

Leakage between pins may occur if the power is turned on while the device has condensation or dirt on it. Make sure the device is dry and clean before supplying power to it.

Fig. 1: Example GND Pattern

RTC - 4553 (SOP-14pin)

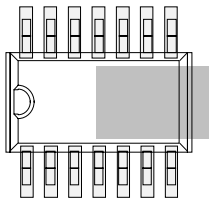
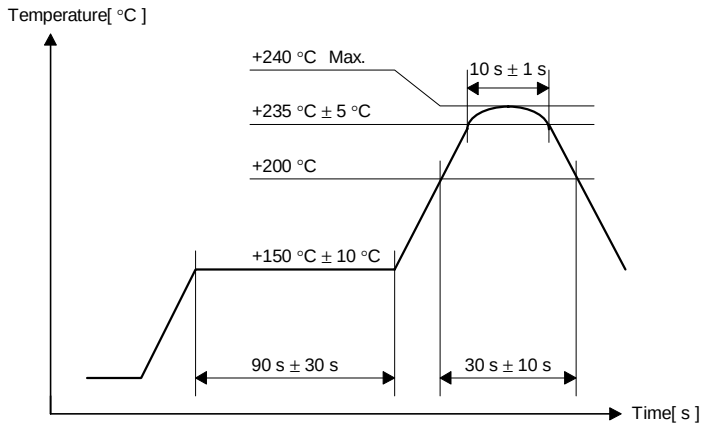


Fig. 2: Soldering Conditions of SMD Products
Air Reflow Profile



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